2014 Xilinx All Programmable客户技术培训

Designing a Custom AXI Peripheral

2014.1

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Introduction

- **What AXI signals do I need and what are their names?**
- **How do I design an AXI peripheral?**
- **How does the Create and Package IP Wizard in the Vivado Design Suite create the custom IP?**
- **Implement custom IP quickly**
  - Wizard eases the creation process

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Objectives

After completing this module, you will be able to:

- List some of the AXI peripheral design approaches
- Describe AXI signal naming conventions
- Identify the transaction logic needed to implement various AXI attachments
- Generate an IP template using the Create and Package IP Wizard

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Talking AXI

- **Talking AXI**
- AXI Backend Signaling Requirements
- Writing a Custom AXI Peripheral from Scratch
- Starting with the Vivado IDE Create and Package IP Wizard
- Summary

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AXI Design – Basic Requirements

- **AXI transaction signaling requirements for custom attachments**
  - Must implement channels needed for attachment implementation
    - Read address channel
    - Read data channel
    - Write address channel
    - Write data channel
    - Write response channel
    - Not all channels may be needed for every design
  - Requirements vary with attachment (gender)
    - Master
    - Slave

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Popular AXI Design Approaches

- **AXI interface is simple**
  - Common IP interface protocol framework common across most design approaches
- **Xilinx supports six types of AXI4 IP**
  - AXI4 Master
  - AXI4 Slave
  - AXI4-Lite Master
  - AXI4-Lite Slave
  - AXI4-Stream Master
  - AXI4-Stream Slave
- **Automatic template generation from Create and Package IP Wizard in the Vivado IDE**

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AXI Design – User Requirements

- **Design approach depends on transaction data phase types**
  - Single data phase (AXI4-Lite)
  - Burst (AXI4)
  - Desired AXI4 interconnect support
- **Attachment interface requirements**
  - Compatible with Xilinx AXI interconnect
  - Specify user IP data width
  - Specify user address width
    - No address for AXI Stream
  - Follows S_AXI_x and M_AXI_x signal naming conventions

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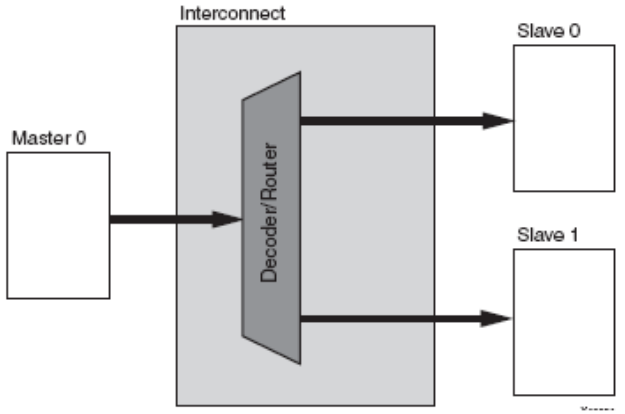
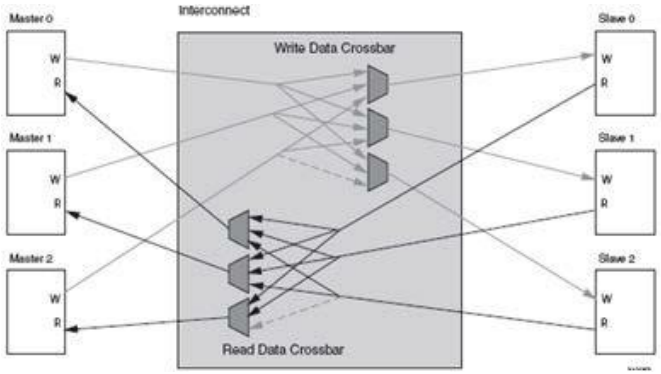
AXI Interconnect

- **Supported in IP integrator as an IP component**
  - "axi_interconnect"
  - Highly configurable
    - Pass Through
    - Conversion Only
    - N-to-1 Interconnect
    - 1-to-N Interconnect
    - N-to-M Interconnect – full crossbar
    - N-to-M Interconnect – shared bus structure
- **Decoupled master and slave interfaces**
- **Point-to-point AXI connection provides simplified interoperability**
- **Reference**
  - *Xilinx AXI Reference Guide* (UG761)



1-to-N Interconnect



N-to-M Interconnect – Full Crossbar

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AXI Backend Signaling Requirements

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AXI Signal Naming Conventions

- **AXI transaction signaling naming requirements for custom attachments**
  - Required by the Vivado IDE IP Packager for proper integration
  - Master attachments
    - M_AXI_
  - Slave attachments
    - S_AXI_
  - Names can later be reassign for uniqueness by using wrappers

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Required Attachment Generic/Parameters

- **VHDL generics or Verilog parameters**
  - Used in block diagram editor to customize peripheral
  - Required by Vivado IDE IP Packager for proper integration
    - C_**x**_AXI_DATA_WIDTH : integer := 32;
      - Width should match interconnect port; typically 32 bits for processor peripherals
    - C_**x**_AXI_ADDR_WIDTH : integer := 4
      - For processor peripherals, varies on address space needed
      - Not needed for streaming AXI port
  - Names typically remain constant to insure configuration ability in IP GUI
  - User-defined parameters are encouraged!

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Required AXI Common Signals

- **Common AXI transaction signal required for all custom attachments**
  - Required by Vivado IDE IP Packager for proper integration
  - Clock
    - S_AXI_ACLK or M_AXI_ACLK
  - Reset
    - S_AXI_ARESETN or M_AXI_ARESETN
  - Names can later be reassigned for uniqueness by using wrappers

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AXI4 Lite Required Attachment Signals

- **AXI4 Lite signals required for Xilinx attachments**
  - Common to slave or master attachment (S_AXI, M_AXI)
    - **x**_AXI_A**x**ADDR – read or write address
    - **x**_AXI_**x**DATA – read or write data
    - **x**_AXI_**x**VALID – address or data is valid from initiator
    - **x**_AXI_**x**READY – address or data acknowledged by target
    - **x**_AXI_**x**RESP – read or write transaction response
    - **x**_AXI_A**x**PROT – read or write transaction address protection
    - **x**_AXI_WSTRB – write channel strobe
  - Master attachments require additional signals (see Notes section)
  - All five AXI channels required
  - User can tie off unused outputs and ignore unused inputs

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AXI4 Full Required Attachment Signals

- **AXI4 Lite signals required for Xilinx attachments**
  - In addition to the AXI4 Lite requirements
  - Common to slave or master attachment (S_AXI, M_AXI)
    - **x**_AXI_**x**ID – requester ID
    - **x**_AXI_A**x**LEN – burst length
    - **x**_AXI_A**x**SIZE – size of each transfer in the burst
    - **x**_AXI_A**x**BURST – burst type
    - **x**_AXI_A**x**LOCK – memory lock type
    - **x**_AXI_A**x**CACHE – memory type
    - **x**_AXI_A**x**QOS – quality of service identifier
    - **x**_AXI_A**x**REGION – memory region identifier
    - **x**_AXI_**x**USER – optional user-defined signals
    - **x**_AXI_**x**LAST – last data phase indicator

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AXI4 Stream Required Attachment Signals

- **AXI4 Stream signals required for Xilinx attachments**
  - Common to slave or master attachment (S_AXIS, M_AXIS)
    - **x**_AXIS_TVALID – data is valid from initiator
    - **x**_AXIS_TDATA – data
    - **x**_AXIS_TSTRB – byte qualifier
    - **x**_AXIS_TLAST – boundary of last packet
    - **x**_AXIS_TREADY – data acknowledged by target
  - Generic/parameters
    - C_S_AXIS_TDATA_WIDTH – data width
  - AXI Stream signal group is mutually exclusive of AXI Full or Lite

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Writing a Custom AXI Peripheral from Scratch

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Starting with a Blank Design

- **Designer is responsible to get everything right**
  - AXI signal naming conventions
  - Include needed AXI signals to attachment
  - Proper response to all channel interface port signals
- **Consider getting a good head start using the Create and Package IP Wizard in the Vivado IDE**

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AXI4 Slave Transaction Implementation

- **AXI4 slave transaction logic required for Xilinx attachments**
  - Ready/valid for all channels
  - Latch target address based on burst type
  - Burst data phase counter (not needed for AXI4 Lite)
  - Transaction response

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AXI4 Master Transaction Implementation

- **AXI4 master transaction logic required for Xilinx attachments**
  - Ready/valid for all channels
  - Transaction initiation logic
  - Logic to emit read and write channel address
  - Read and write data channel logic
    - Send or receive data
    - Response logic
    - Data burst counter
    - Last data detection
  - Error detection and handling logic

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AXI4 Stream Transaction Implementation

- **AXI4 stream transaction logic required for Xilinx attachments**
  - Similar logic for stream master or slave
  - Ready/valid for all channels
  - Packet state machine: start and last data logic
  - Very much application dependent

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Using Xilinx Vivado IDE Create and Package IP Logic as a Starting Point

- **Create and Package IP Wizard in the Vivado IDE creates starting point designs**
  - AXI signal naming conventions
  - Includes needed AXI signals to attachment
  - Transaction logic covered in last three slides
  - Verilog or VHDL source code

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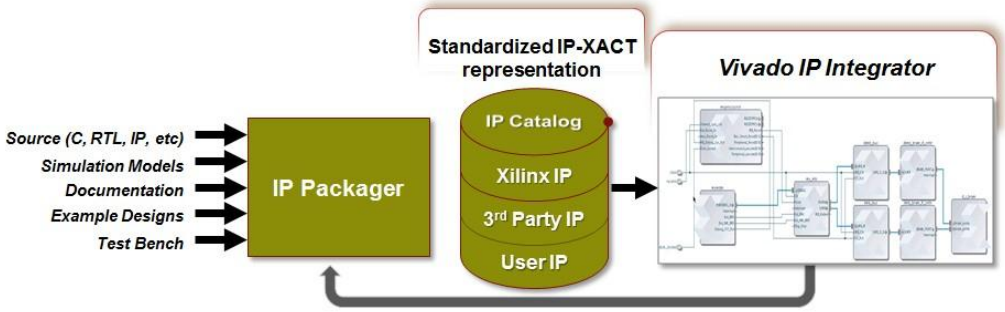
Reuse Custom IP

- **Vivado IP packager**
  - Fully integrated into the Vivado Design Suite
  - Easy to use
  - Enables multiple file types to be packaged into a single structure, including
    - Sources (VHDL, Verilog, C)
    - Constraints
    - Testbenches
    - Documentation
  - Makes user IP available in the extensible IP catalog



- **IPs in the Vivado IP catalog can be used to create IP integrator designs**
- **IP integrator block design can also be packaged as customized IP**

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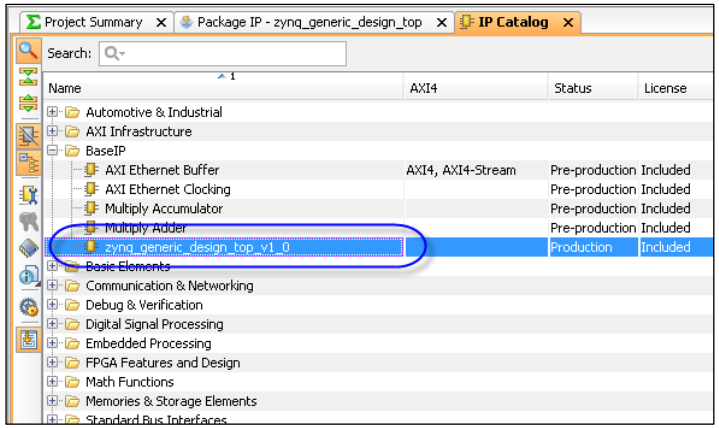
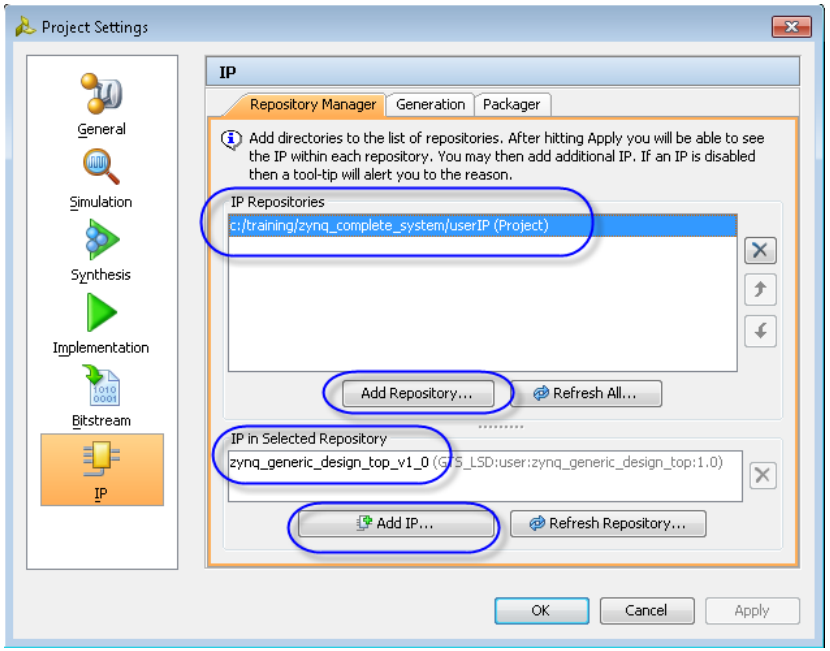
Add New IP to IP Catalog

- **Custom new IP can be added to IP catalog in two ways**
  - **Add to Catalog** in the Review and Package tab will update catalog with new IP automatically
  - **IP Settings** in the IP Catalog window opens repository manager to add new IP or additional IP



- **IP Repository Manager is a GUI**
  - Add repository in which IP exists in zip
  - Select IP from the repository
  - Add IP packaged to IP catalog



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Starting with the Vivado IDE Create and Package IP Wizard

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Vivado IDE Create and Package IP Wizard

- **Package any IP, including AXI to make it available in the Vivado IP catalog**
- **Used to package AXI IP that was written from scratch**
- **Can generate skeleton AXI IP templates**
  - AXI4 Full
  - AXI4 Lite
  - AXI4 Stream
  - Master and slave
  - Recommended design starting point

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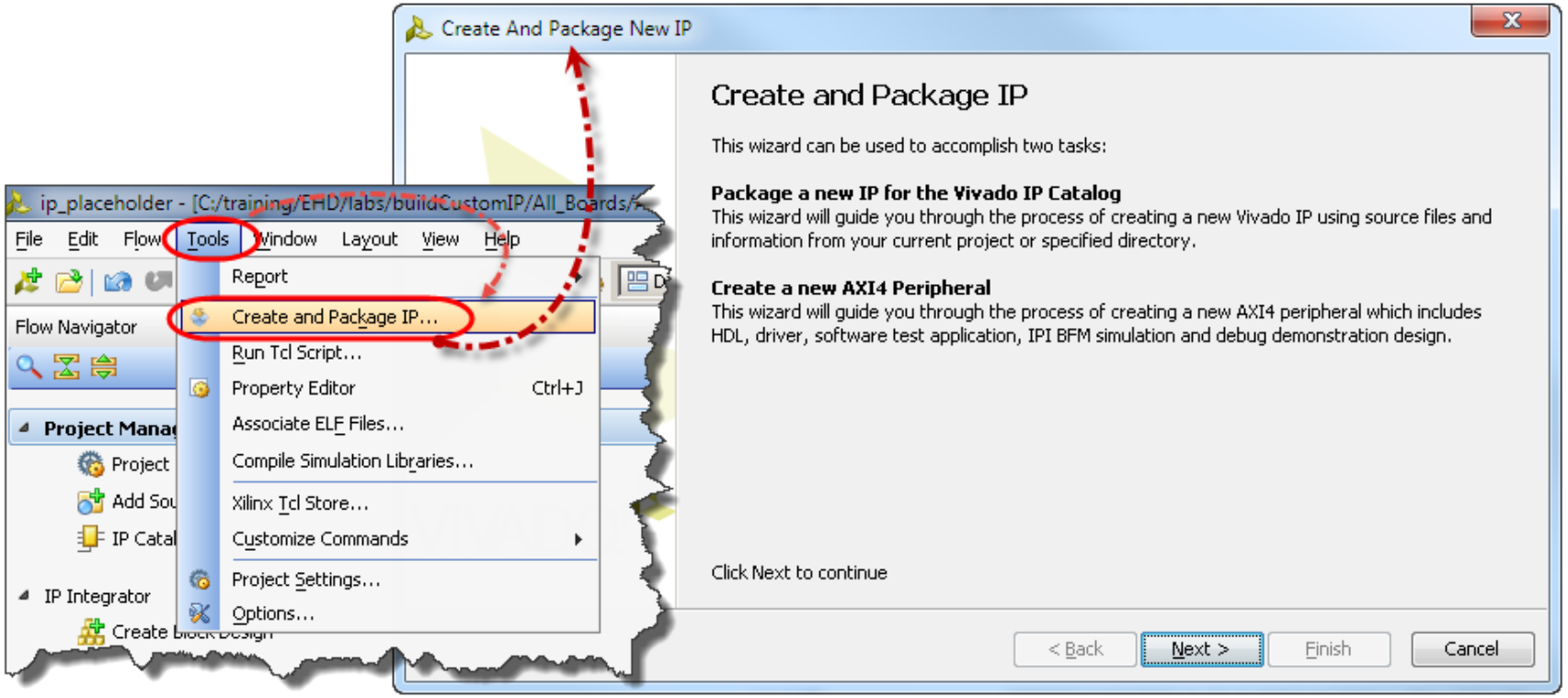
Launching the Wizard



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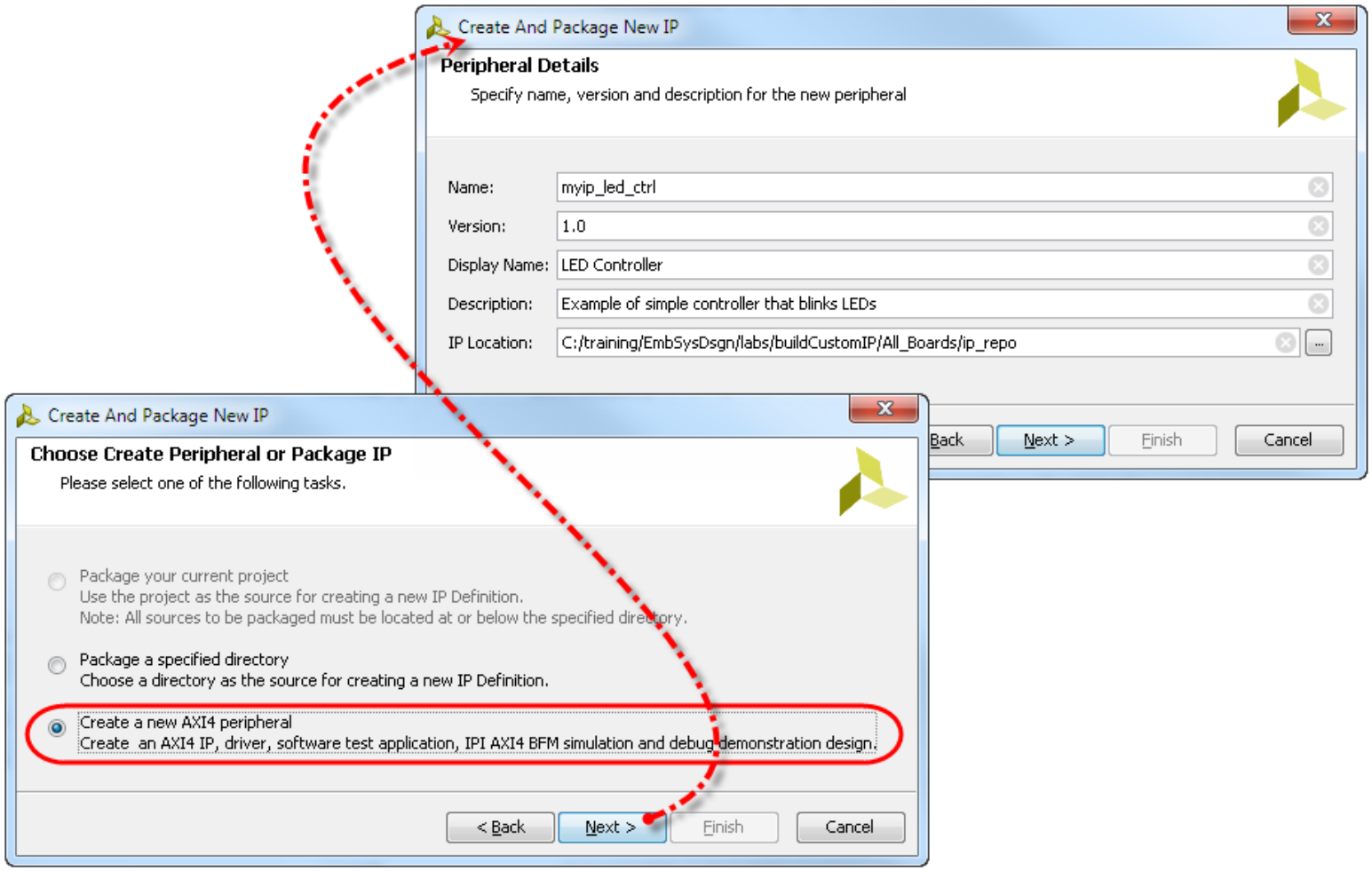
Selecting Create AXI IP Design Template



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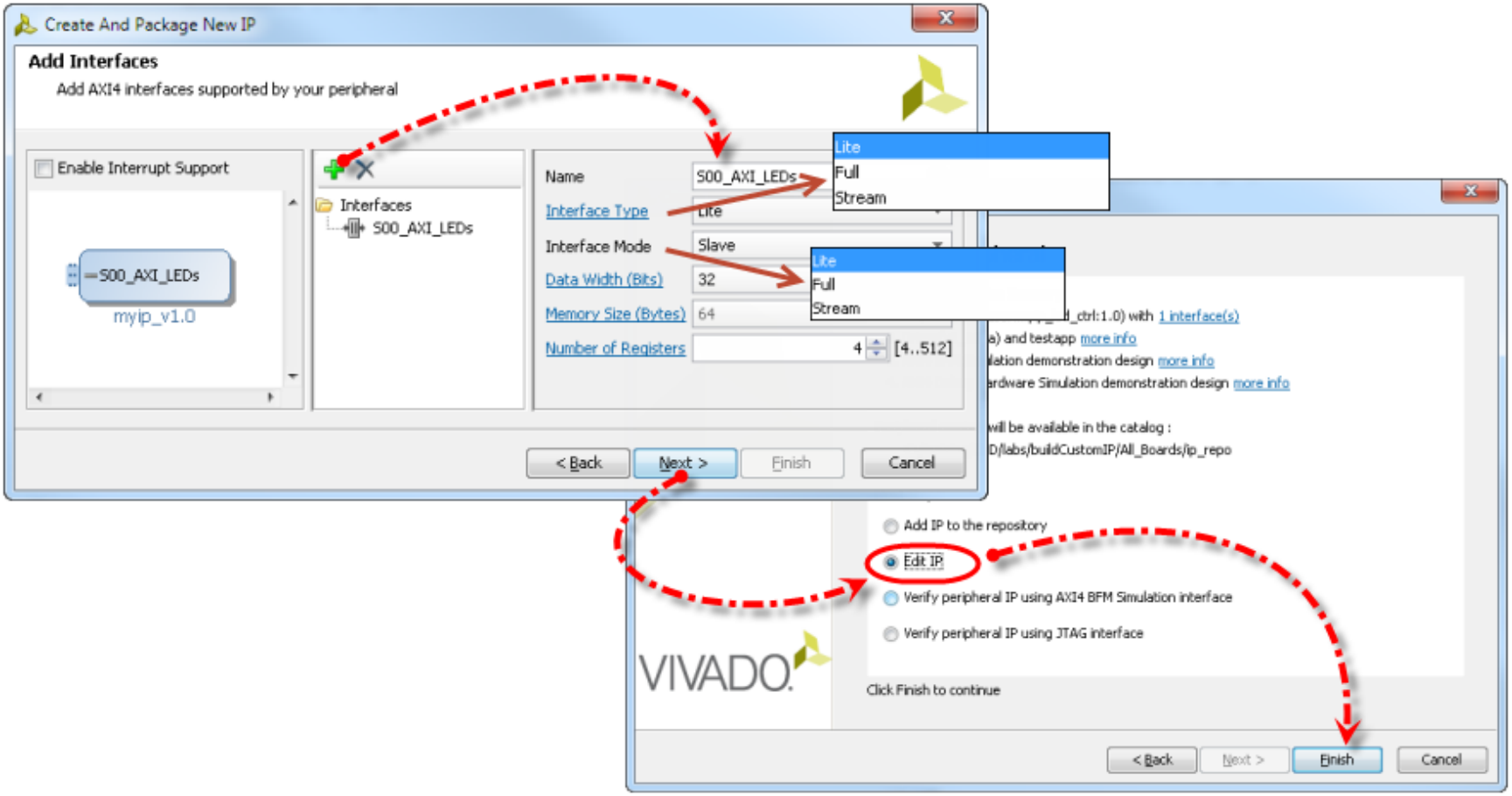
Customizing AXI IP Design Template



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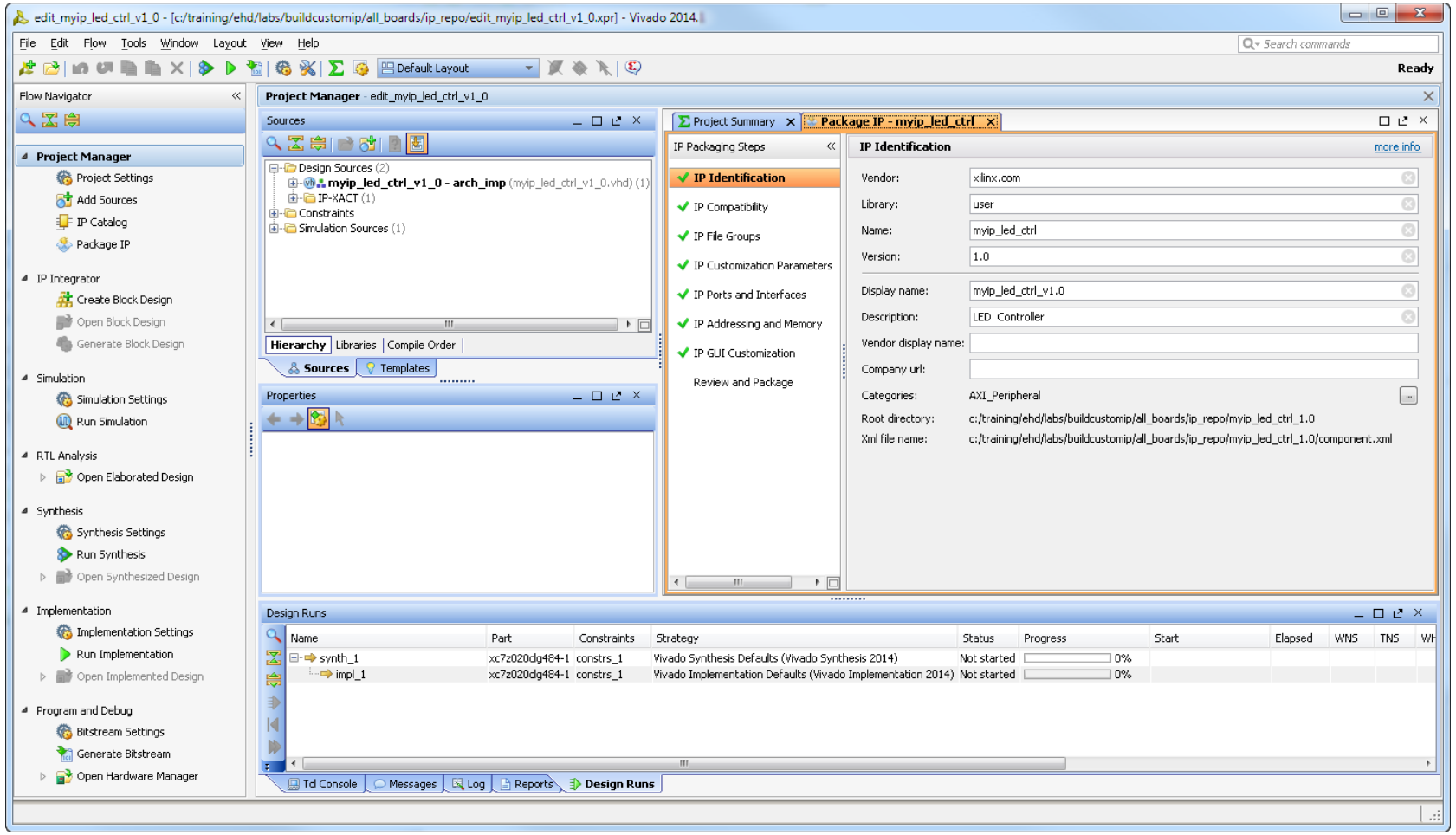
Wizard-Created AXI IP Design Environment



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Apply Your Knowledge

1. List some of the AXI peripheral design approaches

2. Describe AXI signal naming conventions

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Summary

- **AXI attachment approaches include: Lite, Full, and Streaming (both master and slave)**
- **Proper AXI signal naming conventions must be followed**
- **Each attachment has minimal transaction logic design requirements**
- **Create and Package IP Wizard facilitates design efforts**
  - Skeleton AXI templates in Verilog or VHDL
  - Vivado IDE project design environment
  - Xilinx-recommended design flow

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