Basic FPGA Architectures

Objectives

After completing this module, you will be able to:

- Identify the basic architectural resources
  - Look at Virtex™-II FPGA
- List the differences between the Virtex and Spartan Families
  - Virtex: Virtex-II, Virtex-II Pro
  - Spartan: Spartan™-3, Spartan-3E, and Spartan-3A devices
- List the enhanced features of Virtex-4 and Virtex-5 device families
- List the new and enhanced features of the Virtex-6 device family
- List the new and enhanced features of the Spartan-6 device family

Outline

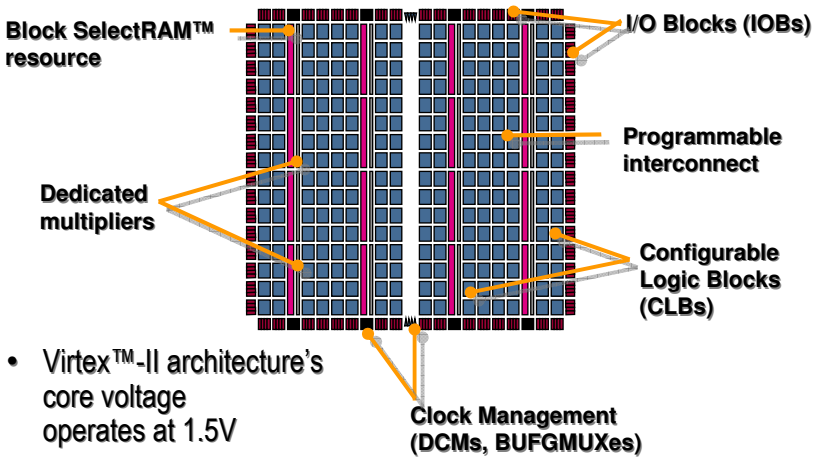
- **Overview**
- Case Study: Virtex-II
  - Logic Resources
  - I/O Resources
  - Memory
  - Clocking
- Other Architectures
- Latest Families
  - Virtex-6 Family
  - Spartan-6 Family
- Summary

Overview

- All Xilinx FPGAs contain the same basic resources
  - Logic Resources
    - Slices (grouped into CLBs)
      - Contain combinatorial logic and register resources
    - Memory
    - Multipliers
  - Interconnect Resources
    - Programmable interconnect
    - IOBs
      - Interface between the FPGA and the outside world
  - Other resources
    - Global clock buffers
    - Boundary scan logic

Virtex-II Architecture

First FPGA Device to include embedded multipliers



- Virtex™-II architecture's core voltage operates at 1.5V

Outline

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- **Virtex-II**
  - Logic Resources
  - I/O Resources
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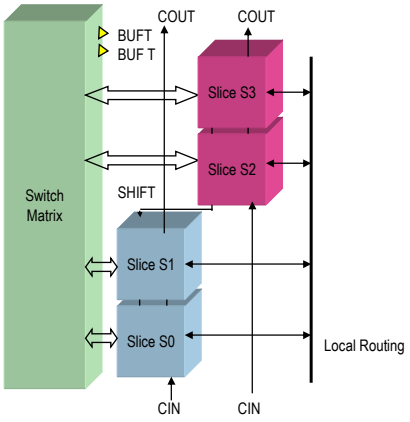
Basic Building Block

Configurable Logic block

- Slices contain logic resources and are arranged in two colums
- A switch matrix provides access to general routing resources
- Local routing provides connection between slices in the same CLB, and it provides routing to neighboring CLBs

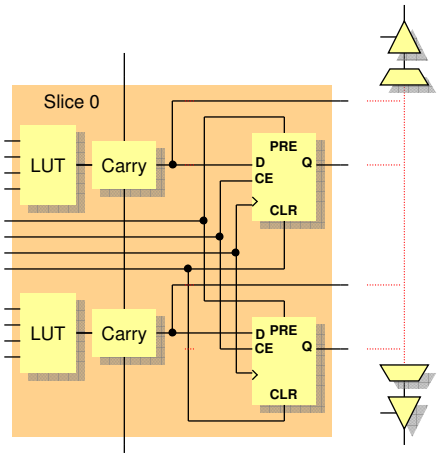


Virtex-II CLB contains four slices

Basic Building Blocks

Simplified Slice Structure

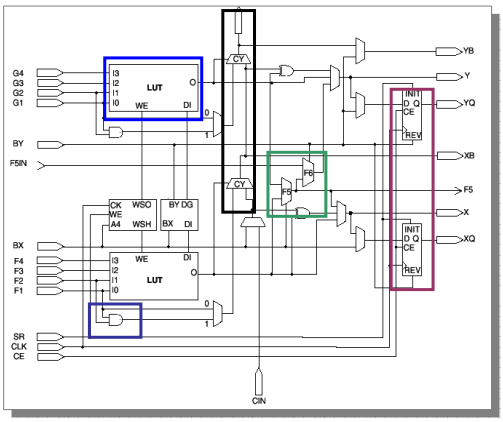
- Each slice has four outputs
  - Two registered outputs, two non-registered outputs
  - Two BUFTs associated with each CLB, accessible by all 16 CLB outputs
- Carry logic runs vertically, up only
  - Two independent carry chains per CLB



The Slice

Detailed Structure

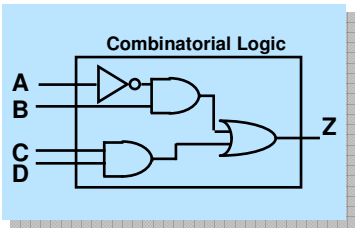
- The next few slides discuss the slice features
  - LUTs
  - MUXF5, MUXF6, MUXF7, MUXF8 (only the F5 and F6 MUX are shown in this diagram)
  - Carry Logic
  - MULT_ANDs
  - Sequential Elements



Combinatorial logic

Boolean logic is stored in Look-Up Tables (LUTs)

- Also called Function Generators (FGs)
- Capacity is limited by the number of inputs, not by the complexity
- Delay through the LUT is constant

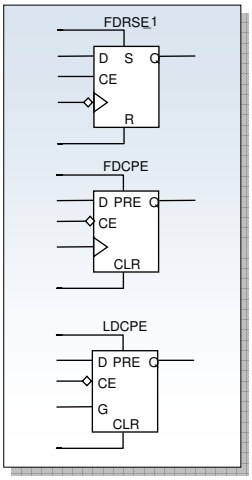


A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Storage Elements

Can be implemented as either flip-flops or latches

- Two in each slice; eight in each CLB
- Inputs come from LUTs or from an independent CLB input
- Separate set and reset controls
  - Can be synchronous or asynchronous
- All controls are shared within a slice
  - Control signals can be inverted locally within a slice



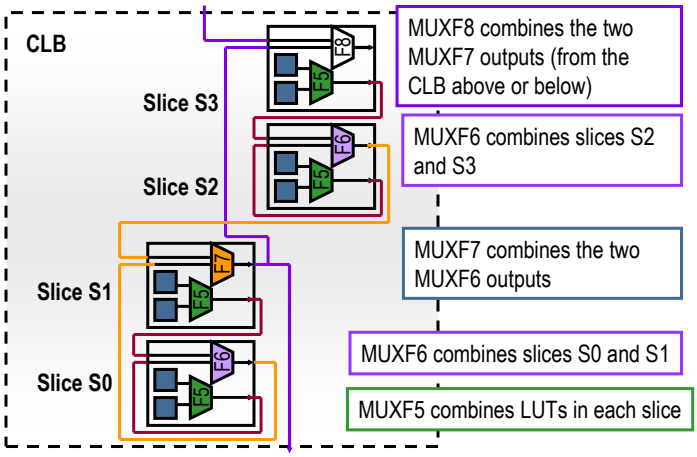
Dedicated Logic

FPGAs contain built-in logic for speeding up logic operations and saving resources

- Multiplexer Logic
  - Connect Slices and LUTs
- Carry Chains
  - Speed up arithmetic operations
- Multiplier AND gate
  - Speed up LUT-based multiplication
- Shift Register LUT
  - LUT-based shift register
- Embedded Multiplier
  - 18x18 Multiplier

Multiplexer Logic

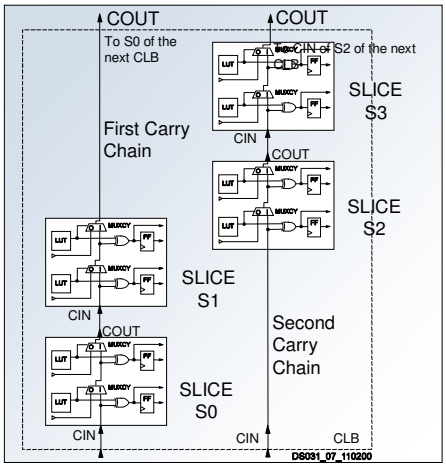
Dedicated MUXes provided to connect slices and LUTs



Carry Chains

Dedicated carry chains speeds up arithmetic operations

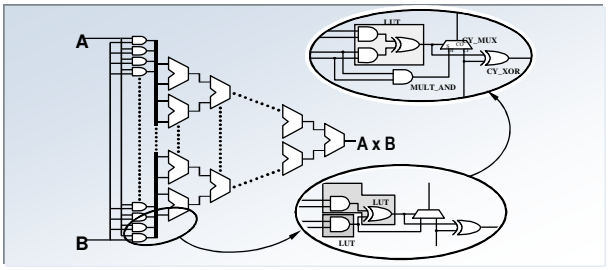
- Simple, fast, and complete arithmetic Logic
  - Dedicated XOR gate for single-level sum completion
  - Uses dedicated routing resources
  - All synthesis tools can infer carry logic



Multiplier AND Gate

Speed up LUT-based multiplication

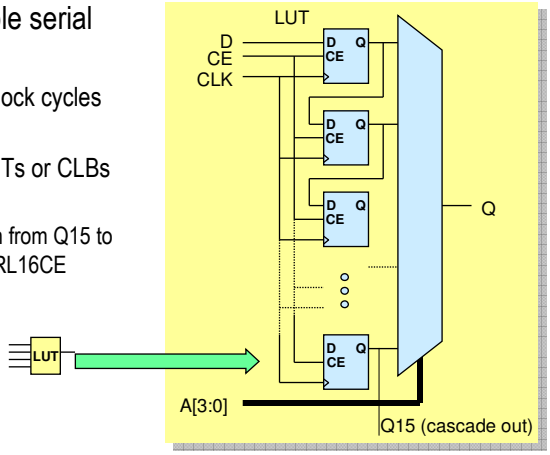
- Highly efficient multiply and add implementation
  - Earlier FPGA architectures require two LUTs per bit to perform the multiplication and addition
  - The MULT_AND gate enables an area reduction by performing the *multiply* and the *add* in one LUT per bit



Shift Register LUT (SRL16CE)

The shift register LUT saves from having to use dedicated registers

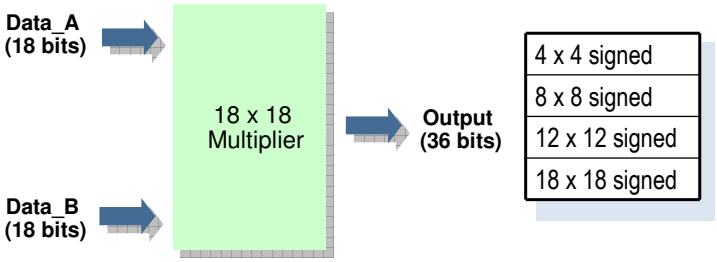
- Dynamically addressable serial shift registers
  - Maximum delay of 16 clock cycles per LUT (128 per CLB)
  - Cascadable to other LUTs or CLBs for longer shift registers
    - Dedicated connection from Q15 to D input of the next SRL16CE
  - Shift register length can be changed asynchronously by toggling address A



Embedded Multiplier Blocks

Saves from having to use LUTs to implement multiplications and increases performance

- 18-bit twos complement signed operation
- Optimized to implement Multiply and Accumulate functions
- Multipliers are physically located next to block SelectRAM™ memory



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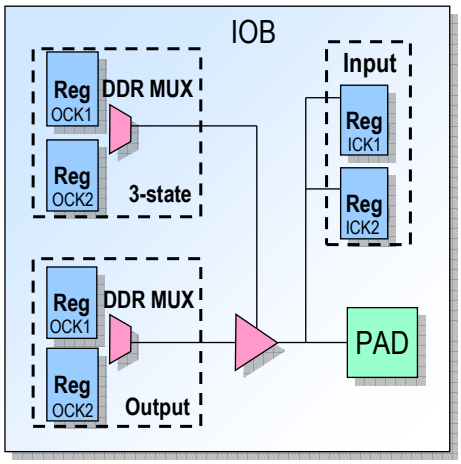
IOB Element

Connects the FPGA design to external components

- Input path
  - Two DDR registers
- Output path
  - Two DDR registers
  - Two 3-state enable DDR registers
- Separate clocks and clock enables for I and O
- Set and reset signals are shared



SelectIO Standard

FPGA I/O pins can be configured to support various standards

- Allows direct connections to external signals of varied voltages and thresholds
  - Optimizes the speed/noise tradeoff
  - Saves having to place interface components onto your board
- Differential signaling standards
  - LVDS, BLVDS, ULVDS
  - LDT
  - LVPECL
- Single-ended I/O standards
  - LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
  - PCI-X at 133 MHz, PCI (3.3V at 33 MHz and 66 MHz)
  - GTL, GTLP
  - and more!

Digital Controlled Impedance (DCI)

- DCI provides
  - Output drivers that match the impedance of the traces
  - On-chip termination for receivers and transmitters
- DCI advantages
  - Improves signal integrity by eliminating stub reflections
    - Occurs when the termination resistor is too far away from the end of the transmission line
    - With DCI, the resistors are as close to the input buffer or output buffer as possible, thereby eliminating stub reflections
  - Reduces board routing complexity and component count by eliminating external resistors
  - Eliminates the effects of temperature, voltage, and process variations by using an internal feedback circuit

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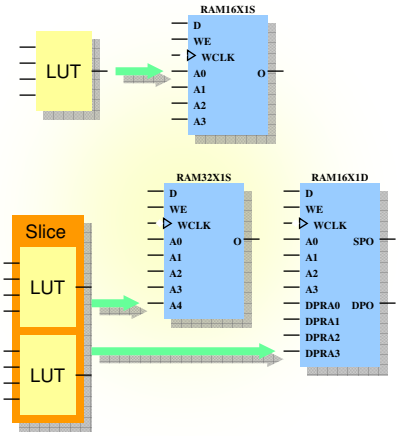
Distributed RAM

Uses a LUT in a slice as memory

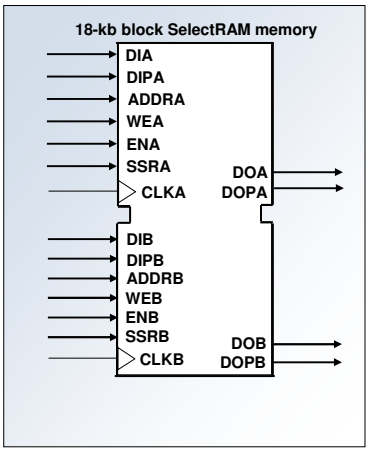
- Synchronous write
- Asynchronous read
  - Accompanying flip-flops can be used to create synchronous read
- RAM and ROM are initialized during configuration
  - Data can be written to RAM after configuration
- Emulated dual-port RAM
  - One read/write port
  - One read-only port
- 1 LUT = 16 RAM bits



Block RAM

Embedded blocks of RAM arranged in columns

- Up to 3.5 Mb of RAM in 18-kb blocks
  - Synchronous read and write
- True dual-port memory
  - Each port has synchronous read and write capability
  - Different clocks for each port
- Supports initial values
- Synchronous reset on output latches
- Supports parity bits
  - One parity bit per eight data bits
- Situated next to embedded multiplier for fast multiply-accumulate operations



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Global Routing

- Sixteen dedicated global clock multiplexers
  - Eight on the top-center of the die, eight on the bottom-center
  - Driven by a clock input pad, a DCM, or local routing
- Global clock multiplexers provide the following:
  - Traditional clock buffer (BUFG) function
  - Global clock enable capability (BUFGCE)
  - Glitch-free switching between clock signals (BUFGMUX)
- Up to eight clock nets can be used in each clock region of the device
  - Each device contains four or more clock regions

Digital Clock Manager (DCM)

- Up to twelve DCMs per device
  - Located on the top and bottom edges of the die
  - Driven by clock input pads
- DCMs provide the following:
  - Delay-Locked Loop (DLL)
  - Digital Frequency Synthesizer (DFS)
  - Digital Phase Shifter (DPS)
- Up to four outputs of each DCM can drive onto global clock buffers
  - All DCM outputs can drive general routing

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Virtex Architectures

Built for high-performance applications

Other Families include

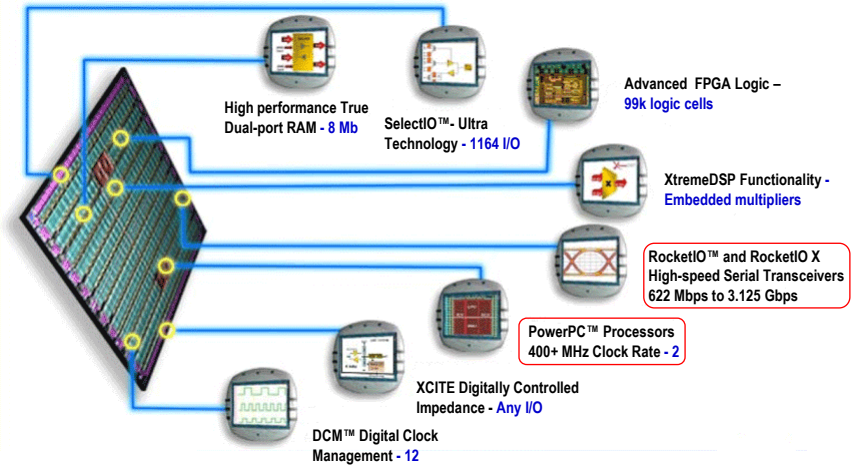
- Virtex-II Pro
- Virtex-4
- Virtex-5

Latest Family include

- Virtex-6

Virtex-II Pro Architecture

Contains embedded Processors and Multi-Gigabit Transceivers



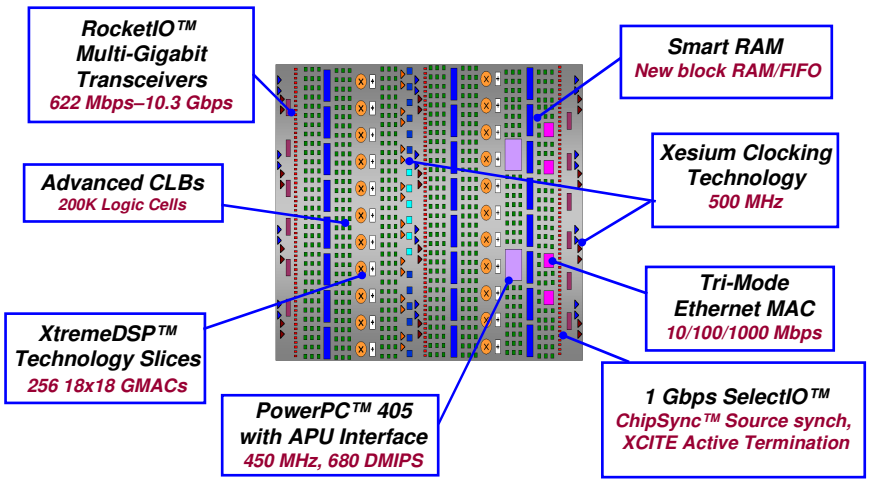
130 nm, 9 layer copper in 300 mm wafer technology

Virtex-4 Family

Advanced Silicon Modular BLock (ASMBL) Architecture
Optimized for logic, Embedded, and Signal Processing

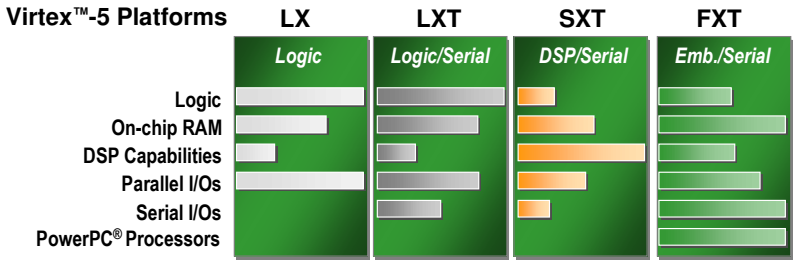
Resource	LX	FX	SX
Logic	14K–200K LCs	12K–140K LCs	23K–55K LCs
Memory	0.9–6 Mb	0.6–10 Mb	2.3–5.7 Mb
DCMs	4–12	4–20	4–8
DSP Slices	32–96	32–192	128–512
SelectIO	240–960	240–896	320–640
RocketIO	N/A	0–24 Channels	N/A
PowerPC	N/A	1 or 2 Cores	N/A
Ethernet MAC	N/A	2 or 4 Cores	N/A

Virtex-4 Architecture

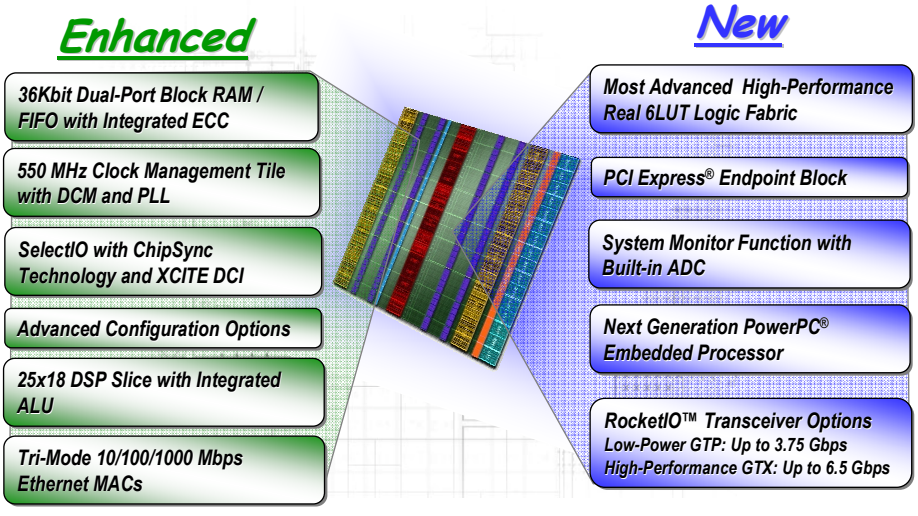


Virtex-5 Family

Optimized for logic, Embedded, Signal Processing, and High-Speed Connectivity



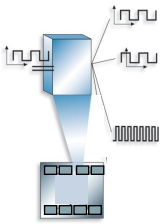
Virtex-5 Architecture



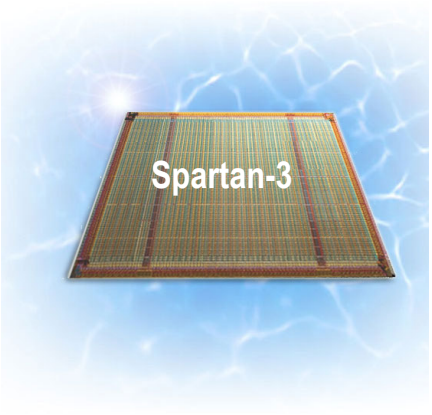
The Spartan-3 Family

Built for high volume, low-cost applications

18x18 bit Embedded Pipelined Multipliers for efficient DSP



Up to eight on-chip Digital Clock Managers to support multiple system clocks



Configurable 18K Block RAMs + Distributed RAM

4 I/O Banks, Support for all I/O Standards including PCI, DDR333, RSDS, mini-LVDS

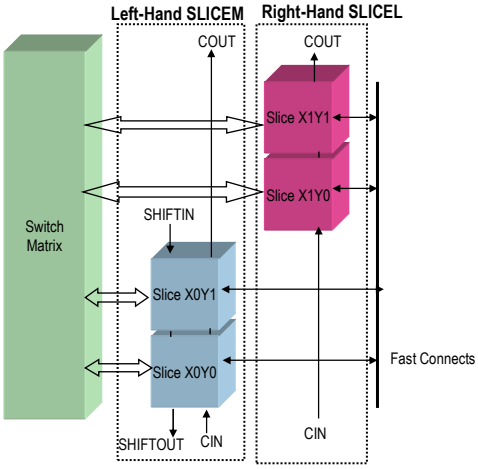
Spartan-3 Family

Based upon Virtex-II Architecture – Optimized for Lower Cost

- Smaller process = lower core voltage
  - .09 micron versus .15 micron
  - Vccint = 1.2V versus 1.5V
- Logic resources
  - Only one-half of the slices support RAM or SRL16s (SLICEM)
  - Fewer block RAMs and multiplier blocks
- Clock Resources
  - Fewer global clock multiplexers and DCM blocks
- I/O Resources
  - Fewer pins per package
  - No internal 3-state buffers
  - Support for different standards
    - New standards: 1.2V LVCMOS, 1.8V HSTL, and SSTL
    - Default is LVCMOS, versus LVTTL

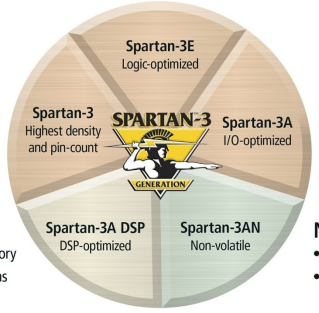
SLICEM and SLICEL

- Each Spartan™-3 CLB contains four slices
  - Similar to the Virtex™-II
- Slices are grouped in pairs
  - Left-hand SLICEM (Memory)
    - LUTs can be configured as memory or SRL16
  - Right-hand SLICEL (Logic)
    - LUT can be used as logic only



Multiple Domain-optimized Platforms

Mainstream
- Broad range of densities, general functionality and targeted specific application solutions
- Lower total system cost while increasing functionality



DSP
- Integrated DSP MACs and expanded memory
- Optimized for signal processing applications

Non-Volatile
- Combines leading-edge technology FPGAs & Flash technologies
- New evolution in security, protection and functionality

Spartan-3E Features

- More gates per I/O than Spartan-3
- Removed some I/O standards
  - Higher-drive LVCMOS
  - GTL, GTLP
  - SSTL2_II
  - HSTL_II_18, HSTL_I, HSTL_III
  - LVDS_EXT, ULVDS
- DDR Cascade
  - Internal data is presented on a single clock edge
- 16 BUFGMUXes on left and right sides
  - Drive half the chip only
  - In addition to eight global clocks
- Pipelined multipliers
- Additional configuration modes
  - SPI, BPI
  - Multi-Boot mode

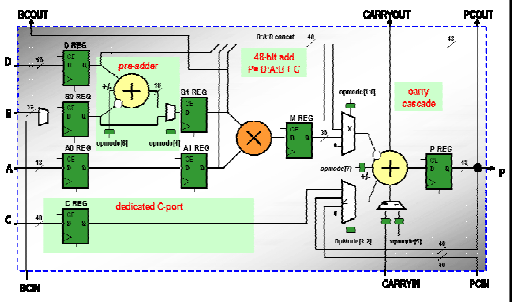
Spartan-3A DSP Features

- Increased amount of block memory (BRAM)
  - 1512K of S3A1800 vs 648 K of S3E1600
- More XtremeDSP DSP48A slices
  - Replaces Embedded multiplier of Spartan-3E
    - 3400A – 126 DSP48As
    - 1800A – 84 DSP48As

Spartan-3A DSP
Tuning DSP Performance

- Integrated XtremeDSP Slice
  - Application optimized capacity
  - Integrated pre-adder optimized for filters
  - 250 MHz operation, standard speed grade
  - Compatible with Virtex-DSP

XtremeDSP DSP48A Slice



- Increased memory capacity and performance
  - Also important for embedded processing, complex IP, etc

DSP48 Comparison

Function	DSP48	DSP48E	DSP48A	Benefit
Multiplier	18 x 18	25 x 18	18 x 18	Reduces FPGA resource needs for DSP algorithms.
Pre-Adder	No	No	Yes	Reduces the critical path timing in FIR filter applications better performance. Important in FIR filter construction.
Cascade Inputs	One	Two	One	Enables fast data path chaining of DSP48 blocks for larger filters.
Cascade Output	Yes	Yes	Yes	Enables fast data path chaining of DSP48 blocks for larger filters.
Dedicated C input	No	Yes	Yes	The C input supports many 3-input mathematical functions, such as 3-input addition and 2-input multiplication with a single addition and the very valuable rounding of multiplication away from zero.
Adder	3 input 48 bit	3 input 48 bit	2 input 48 bit	Supports simple add and accumulate functions.
Dynamic Opmodes	Yes	Yes	Yes	One DSP48 can provide more than one function.. Multiply, Multiply-add, multiply-accumulate etc.
ALU Logic Functions	No	Yes	No	Similar to the ALU of a microprocessor. Enables the selection of ALU function on a clock cycle basis Enables multiple functions to be selected. (Add, Subtract, or Compare)
Pattern Detect	No	Yes	No	This feature supports convergent rounding, underflow/overflow detection for saturation arithmetic, and auto-resetting counters/accumulators.
SIMD ALU Support	No	Yes	No	Enables parallel ALU operations on multiple data sets.
Carry Signals	Carry In	Carry In & Out	Carry In & Out	Supports fast carry functions between DSP blocks. Often a speed limiting path.

Spartan-3A Device Table

	Spartan-3	Spartan-DSP	
	Spartan-3A	Spartan-3A DSP	
	XC3S1400A	XC3SD1800A	XC3SD3400A
XtremeDSP DSP48A Slices	-	84	126
Dedicated Multipliers	32	DSP48As	DSP48As
Block Ram Blocks	32	84	126
Block RAM (Kb)	576	1,512	2,268
Distributed RAM (Kb)	176	260	373
FFs/LUTs	22,528	33,280	47,744
Logic Cells	25,344	37,440	53, 712
DCMs	8	8	8
Max Diff I/O Pairs	227	227	213
CS484 19x19mm (0.8mm pitch)	-	309	309
*FG676 27x27mm (1.0mm pitch)	502	519	469

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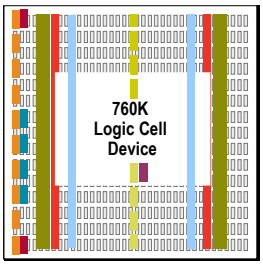
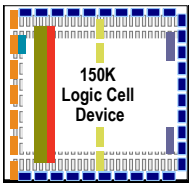
Architecture Alignment

Virtex-6 FPGAs



Spartan-6 FPGAs



Common Resources

- LUT-6 CLB
- BlockRAM
- DSP Slices
- High-performance Clocking
- Parallel I/O
- HSS Transceivers*
- PCIe® Interface

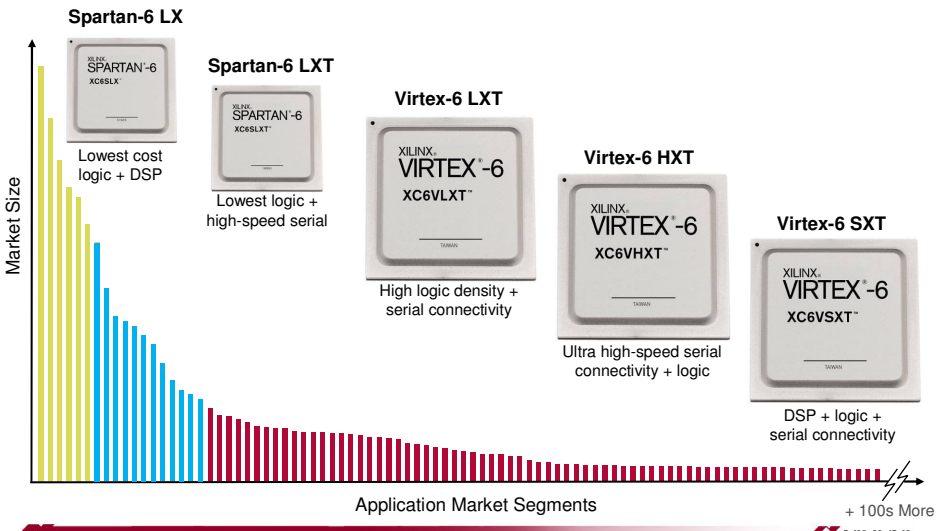
- FIFO Logic
- Tri-mode EMAC
- System Monitor

- Hardened Memory Controllers
- 3.3 Volt compatible I/O

*Optimized for target application in each family

Enables IP Portability, Protects Design Investments

Addressing the Broad Range of Technical Requirements



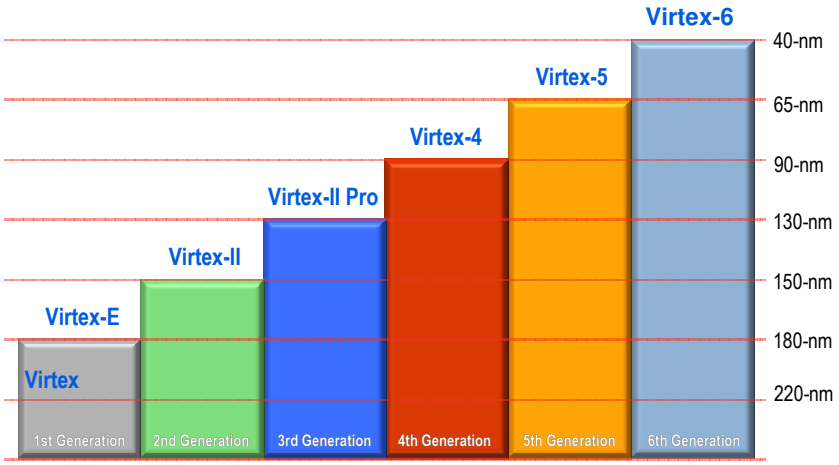
Designers Eccentrics

- Higher System Performance
  - More design margin to simplify designs
  - Higher integrated functionality
- Lower System Cost
  - Reduce BOM
  - Implement design in a smaller device & lower speed-grade
- Lower Power
  - Help meet power budgets
  - Eliminate heat sinks & fans
  - Prevent thermal runaway

Outline

- Overview
- Virtex-II Architecture
  - Slice Resources
  - I/O Resources
  - Memory
  - Clocking
- Other Architectures
- **Latest Families**
  - Virtex-6 Family
  - Spartan-6 Family
- Summary

Virtex® Product & Process Evolution



Delivering Balanced Performance, Power, and Cost

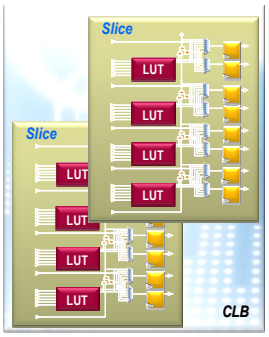
Strong Focus on Power Reduction

- Static Power Reduction
  - Higher distribution of low leakage transistors
- Dynamic Power Reduction
  - Reduced capacitance through device shrink
- Reduced Core Voltage Devices Lower Overall Power
  - VCCINT = 0.9V option allows power / performance tradeoff
- I/O Power Improvements
  - Dynamic termination
- System Monitor
  - Allows sophisticated monitoring of temperature and voltage

Up to 50% Power Reduction vs. Previous Generation

Virtex-6 Logic Fabric

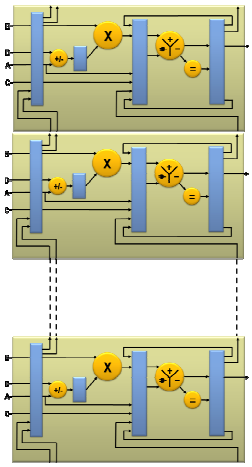
- Virtex-6 Configurable Logic Block (CLB)
  - Each CLB contains two slices
  - Each slice contains four 6-input Lookup Tables (6LUT)
- Slices implement logic functions (slice_l)
- Slices for memories and shift registers (slice_m)
- LUT6 implements
  - All functions of up to 6 variables
  - Two functions of up to 5 or less variables each
  - Shift registers up to 32 stages long
  - Memories of 64 bits
    - Multiple configurations within a slice



Power Consumption Benefits	Performance Benefits	Cost Benefits
• Shift register mode greatly reduces power consumption over FF implementation	• Increased ratio of slice_m – memories available closer to the source or target logic	• Can pack logic and memory functions more efficiently

Higher DSP Performance

- Most advanced DSP architecture
  - New optional pre-adder for symmetric filters
  - 25x18 multiplier
    - High resolution filters
    - Efficient floating point support
  - ALU-like second stage enables mapping of advanced operations
    - Programmable op-code
    - SIMD support
    - Addition / Subtraction / Logic functions
  - Pattern detector
- Lowest power consumption
- Highest DSP slice capacity
  - Up to 2K DSP Slices



Virtex®-6 LXT / SXT FPGAs

Part Number		LX75T	LX130T	LX195T	LX240T	LX365T	LX550T	LX760	SX315T	SX475T
Logic Cells		74.5K	128K	200K	241K	364K	550K	759K	315K	476K
CLB Flip-Flops		93.1K	160K	250K	301K	455K	687K	948K	394K	595K
Maximum Distributed RAM (Kbits)		1,045	1,740	3,040	3,650	4,130	6,200	8,280	5,090	7,640
Block RAM/FIFO w/ ECC (36Kbits each)		156	264	344	416	416	632	720	704	1,064
Total Block RAM (Kbits)		5,616	9,504	12,384	14,976	14,976	22,752	25,920	25,344	38,304
Mixed Mode Clock Managers (MMCM)		6	10	10	12	12	18	18	12	18
DSP48E1 Slices		288	480	640	768	576	864	864	1,344	2,016
PCI Express® Interface Blocks		1	2	2	2	2	2	0	2	2
10/100/1000 Ethernet MAC Blocks		4	4	4	4	4	4	0	4	4
GTX Low-Power Transceivers		12	20	20	24	24	36	0	24	36
Package	Area (Pitch)	Maximum User I/O: Select IO™ Interface Pins (GTX Transceivers)								
FF484	23 x 23 mm (1.0 mm)	240 (8)	240 (8)							
FF784	29 x 29 mm (1.0 mm)	360 (12)	400 (12)	400 (12)	400 (12)					
FF1156	35 x 35 mm (1.0 mm)		600 (20)	600 (20)	600 (20)	600 (20)				
FF1759	42.5 x 42.5mm (1.0 mm)				720 (24)	720 (24)	840 (36)		720 (24)	840 (36)
FF1760	42.5 x 42.5mm (1.0 mm)						1,200 (0)	1,200 (0)		

* Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

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- Overview
- Virtex-II Architecture
  - Slice Resources
  - I/O Resources
  - Memory
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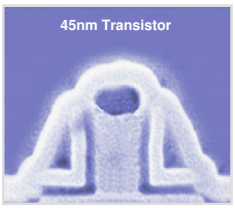
  - Spartan-6 Family
- Summary

Spartan-6

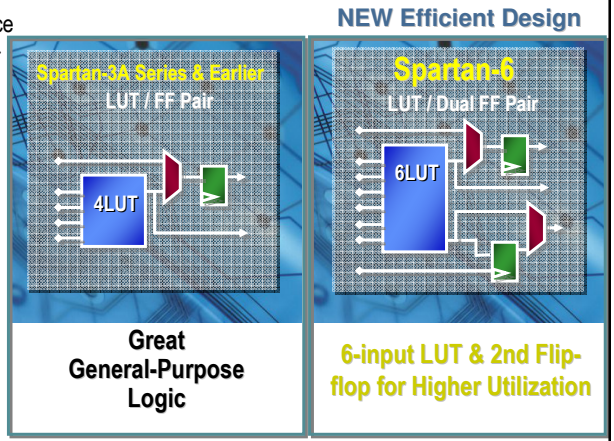
- Next Generation 45nm Spartan Family
  - Increased performance & density
  - Evolutionary feature enhancements
  - Dramatic cost & power reductions
- Two Silicon Platforms
  - LX: Cost optimized Logic, Memory
  - LXT: LX features plus High-Speed Serial Connectivity
  - More unified & integrated with Virtex



Delivering the Optimal Balanced of Cost, Power & Performance

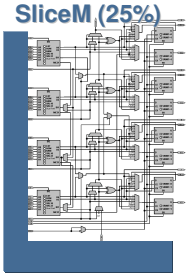
Spartan-6 Logic Evolution
Higher Performance, Increased Utilization

- Modified Virtex 6-input LUT
  - 4 additional flip-flops per slice
  - Higher utilization for register intensive designs
- Efficient & Capable
  - Logic
  - Arithmetic functions
  - Distributed RAM & shift registers
  - Interconnect
- Up to 25% Higher Performance



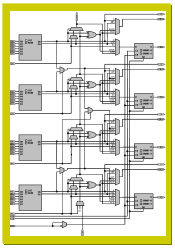
Spartan-6 CLB Logic Slices

SliceM (25%)



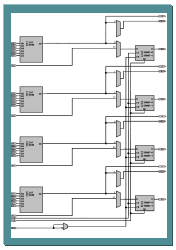
- LUT6
- 8 Registers
- Carry Logic
- Wide Function Muxes
- Distributed RAM / SRL logic

SliceL (25%)



- LUT6
- 8 Registers
- Carry Logic
- Wide Function Muxes

SliceX (50%)



- LUT6
- Optimized for Logic
- 8 Registers

Slice mix chosen for the optimal balance of Cost, Power & Performance

Spartan-6 Lowest Total Power

- Static power reductions
  - Process & architectural innovations
- Dynamic power reduction
  - Lower node capacitance & architectural innovations
- More hard IP functionality
  - Integrated transceivers & other logic reduces power
  - Hard IP uses less current & power than soft IP
- Lower IO power
- Low power option -1L reduces power even further
- Fewer supply rails reduces power

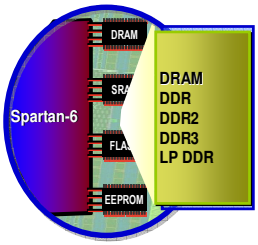
Spartan-6 Hard Memory Controller

- New Hard Block Memory Controller
  - Up to 4 controllers per device
- Why a Hard Memory Block?
  - Very common design component
  - Multiple customer benefits

Customer Requests	Spartan-6 Hard Block Memory Controller Benefits
Higher performance	• Up to 800 Mbps
Lower cost	• Saves soft logic, smaller die
Lower power	• Dedicated logic
Easier designs	• Timing closure no longer an issue • Configurable MultiPort user interface • CoreGen/MIG wizard & EDK support

Memory Controller

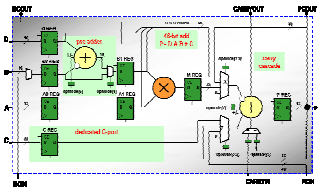
- Only low cost FPGA with a “hard” memory controller
- Guaranteed memory interface performance providing
  - Reduced engineering & board design time
  - DDR, DDR2, DDR3 & LP DDR support
  - Up to 12.8Mbps bandwidth for each memory controller
- Automatic calibration features
- Multiport structure for user interface
  - Six 32-bit programmable ports from fabric
  - Controller interface to 4, 8 or 16 bit memories devices



Integrated DSP Slice

- 250 MHz implementation
  - Fast multiplier & 48 bit adder
  - ASIC-like performance
- Input and output registers for higher speed

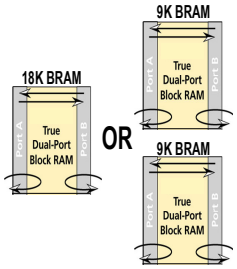
XtremeDSP DSP48A1 Slice



Optimizes FIR filter applications

Better, More BRAM

- More Block RAMs
  - 2x higher BRAM to Logic Cell ratio than Spartan-3A platform
- More port flexibility
  - 18K can be split into two 9K BRAM blocks and can be independently addressed
- Improves buffering, caching & data storage
  - Excellent for embedded processing, communication protocols
  - Enables DSP blocks to provide more efficient video and surveillance algorithms
- Lower Static Power



Compare to Spartan-3A

Twice the Capabilities, Half the Power, Hard Blocks!

Feature	Extended Spartan-3A (90nm)	Spartan-6 (45nm)
Logic Cells (Kbit)	Up to 55K	Up to 150K
LUT Design	4-input LUT + FF	6-input LUT + 2FF
Block RAM (Mbit)	Up to 2 Mbit	Up to 5 Mbit
Transceiver Count / Speed	no	Up to 8 / Up to 3.125 Gbps
Voltage Scaling	No (1.2V only)	Yes (1.2V, 1.0V)
Static Power (typ mW)	11 mW (smallest density)	Up to 60% less!
Memory Interface	400 Mbps	DDR3 800 Mbps
Max Differential IO	640 Mbps	1050 Mbps
Multipliers/DSP	Up to 126 Multipliers / DSP	Up to 184 DSP48 Blocks
Memory Controllers	no	Up to 4 Hard Blocks
Clock Management	DCM Only	DCM & PLL
PCI Express Endpoint	no	Yes, Gen 1
Security	Device DNA Only	Device DNA & AES

Spartan-6 LX / LXT FPGAs

Part Number		LX4	LX9	LX16	LX25	LX45	LX100	LX150	LX25T	LX45T	LX100T	LX150T
Logic Cells		3.4K	9K	15K	24K	43K	101K	147K	24K	43K	101K	147K
CLB Flip-Flops		4.2K	11K	18K	30K	54K	126K	184K	28K	54K	126K	184K
Maximum Distributed RAM (Kbits)		32	90	136	228	401	975	1,358	228	401	975	1,385
Block RAM (18K bits each)		8	32	32	52	116	268	268	52	116	268	268
Total Block RAM (Kbits)		144	576	576	936	2,088	4,824	4,824	936	2,088	4,824	4,824
Clock Manager Tiles (CMT)		1	2	2	2	4	6	6	2	4	6	6
DSP48A1 Slices		4	16	32	38	58	182	182	38	58	182	182
PCI Express® Endpoint Block		–	–	–	–	–	–	–	1	1	1	1
Memory Controller Blocks		0	2	2	2	2	4	4	2	2	4	4
GTP Low-Power Transceivers		–	–	–	–	–	–	–	2	4	8	8
Package	Area (Pitch)	Maximum User I/O: Select IO™ Interface Pins (GTP transceivers)										
TQG144	20 x 20 mm (0.5 mm)	100	100									
CSG225	13 x 13 mm (0.8 mm)	120	160	160	160							
FTG256	17 x 17 mm (1.0 mm)			186	186							
CSG324	15 x 15 mm (0.8 mm)		200	232	226				190 (2)	190 (4)		
FGG484	23 x 23 mm (1.0 mm)				264	319	341	341	250 (4)	296 (4)	296 (4)	296 (4)
FGG676	27 x 27 mm (1.0 mm)					370	498	498		370 (4)	396 (8)	396 (8)

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** All memory controller support x16 interface, except in CS225 package where x8 only is supported

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Summary

Virtex-II contains Logic, I/O, Memory, and Clocking Resources

- Virtex-II Logic Resources
  - CLBs which are made up of slices that contain
    - LUTs – can be configured as shift registers or memory
    - Storage elements (flip-flops or latches)
    - Dedicated Logic for speeding up logic operations
  - Embedded Multipliers
- Virtex-II I/O resources
  - SelectIO™ enables communication across multiple standards
  - DCI reduces board complexity be reducing component count
- Virtex™-II memory resources
  - Distributed SelectRAM™ resources and distributed SelectROM (uses CLB LUTs)
  - 18-kb block SelectRAM resources
- Virtex-II Clocking Resources
  - Dedicated global clock lines
  - Digital Clock Managers

Summary

Virtex-II is the basis for subsequent architectures

- Virtex Architectures designed for high-performance applications
  - Virtex-II Pro included PowerPC and RocketIO hard cores enabling embedded processing and high-speed data exchange
  - Virtex-4 introduced ASMBL architecture with three sub-families LX (logic), SX (DSP), and FX (embedded)
  - Virtex-5 introduced 6-input LUT, 36 Kb BRAM and four families LX, LXT, SXT, and FXT
- Spartan architectures designed for low-cost, high-volume applications
  - Matured families include Spartan-3, Spartan-3E, Spartan-3A, Spartan-3AN, Spartan-3A DSP

Summary

- Latest families aligns two architectures- Virtex and Spartan by introducing Virtex-6 and Spartan-6
  - FIFO, Tri-Mode EMAC, and System Monitors are unique to Virtex-6
  - Hardened memory controllers and 3.3v compatible I/Os are unique to Spartan-6
- Both families significantly reduces power consumption through new technology, creative architecture enhancements, and new hardened functional blocks
- Spartan-6 has LX and LXT devices
- Virtex-6 has LXT, SXT, and HXT devices

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